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Description

METHOD FOR FORMING A DEEP TRENCH CAPACITOR BURIED PLATE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method of forming a deep trench capacitor buried plate, and more particularly, to a method for preventing the doped ions from diffusing to the collar region and for avoiding increasing the critical dimension of the deep trench.

[0003] 2. Description of the Prior Art

[0004] As very large scale integration (VLSI) technologies develop, the dimension of the semiconductor elements becomes more and more tiny than before. However, the short channel effect is an obstacle to increase the semiconductor element integration. Before now, some methods are proposed to prevent the short channel effect, such as reducing the thickness of the gate oxide layer or in-

creasing the doped concentration. But these methods lead to some disadvantages, such as lower reliability and lower rate. As a result, a vertical transistor design, which is able to increase the integration, is highly evaluated. Take dynamic random access memory (DRAM) as an example; a deep trench memory integrates the storage capacitor, or even the gate, source, and drain of the transistor into the trench, such that the integration is effectively increased.

[0005] Refer to Fig. 1 to Fig. 4, which are schematic diagrams illustrating a method of forming a deep trench capacitor buried plate according to the prior art. As shown in Fig. 1, first a substrate 10 is provided, and a pad oxide layer 12 and a pad nitride layer 14 are deposited on the substrate 10 in turn. Then a deep trench 16 is formed in the substrate 10.

[0006] As shown in Fig. 2, an arsenic silicate glass (ASG) layer 18 is deposited on the inner wall of the deep trench 16, and a sacrificial layer (not shown in Fig. 2) is deposited to fill up the deep trench 16. Then the sacrificial layer (not shown) is etched back to expose a portion of the arsenic silicate glass layer 18. Afterward, an etching process is performed to remove the exposed arsenic silicate glass layer 18 such that a collar region 20 is formed in the deep trench 16. Fi-

nally another etching process is performed to remove the remaining sacrificial layer (not shown).

[0007] As shown in Fig. 3, a deposition process is performed by use of TEOS (tetra-ethyl-ortho-silicate) as a precursor to form a TEOS layer 22 on the inner wall of the deep trench 16. Then a thermal process is performed to diffuse the arsenic ions of the arsenic silicate glass layer 18 into the substrate 10, such that a doped region 24, serving as a buried plate, is formed.

[0008] Finally as shown in Fig. 4, an etching process is performed to remove the TEOS layer 22 and the arsenic silicate glass layer 18 as well to carry out the deep trench capacitor buried plate.

[0009] As has been pointed out, the prior art method of forming the deep trench capacitor buried plate utilizes a TEOS layer as a barrier layer, and a thermal process is performed to diffuse the arsenic ions into the substrate such that a doped region, serving as a buried plate, is formed. However, since TEOS has poor step coverage ability, a void will easily occur in the opening of the deep trench as the dimension decreases. In addition, as shown in Fig. 3, the TEOS layer 22 does not afford good results as a barrier layer, thus the arsenic ions will easily pass through the

TEOS layer 22 and diffuse into the collar region 22. The arsenic ions in the collar region 22 will cause current leakages of the capacitor.

[0010] Moreover, the pad oxide layer and the TEOS layer are both composed of silicon oxide, as a consequence when an etching process is performed to remove the TEOS layer, some pad oxide layer will be removed as well. The removal of the pad oxide layer would increase the critical dimension of the deep trench, and further lead to a short circuit between neighboring deep trenches.

SUMMARY OF INVENTION

[0011] It is therefore a primary objective of the claimed invention to provide a method of forming a deep trench capacitor buried plate for solving the above-mentioned problems.

[0012] According to the claimed invention, a method forming a deep trench capacitor buried plate is disclosed. The method of the present invention comprises: providing a substrate having a pad oxide layer and a pad nitride layer thereon, the pad oxide layer and the pad nitride layer having at least an opening; performing a dry etching process for forming a deep trench in the substrate via the opening; depositing a doped silicate glass film on an inner wall of the deep trench; filling a sacrificial layer into the

deep trench; removing a portion of the sacrificial layer for exposing parts of the doped silicate glass film; performing an etching process to remove the exposed doped silicate glass film and a portion of the pad nitride layer for forming a recess; removing the remaining sacrificial layer; depositing a silicon nitride layer on the inner wall of the deep trench; performing a diffusing process for forming a doped region at a bottom of the trench; removing the silicon nitride layer; and removing doped silicate glass film. The silicon nitride layer serves as a barrier layer for preventing ions of the doped silicate glass film from diffusing to a collar region of the deep trench.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0014] Fig. 1 to Fig. 4 are schematic diagrams illustrating a method of forming a deep trench capacitor buried plate according to the prior art.

[0015] Fig. 5 to Fig. 8 are schematic diagrams illustrating a method of forming a deep trench capacitor buried plate

according to the present invention.

DETAILED DESCRIPTION

[0016] Refer to Fig. 5 to Fig. 8, which are schematic diagrams illustrating a method of forming a deep trench capacitor buried plate according to the present invention. As shown in Fig. 5, a substrate 50 is provided, and a pad oxide layer 52 and a pad nitride layer 54 are deposited on the substrate 50 in turn. Then a dry etching process is performed to form a deep trench 56 in the substrate 50.

[0017] As shown in Fig. 6, a chemical vapor deposition (CVD) process is performed to form an arsenic silicate glass film 58 on the inner wall of the deep trench 56. Then a sacrificial layer (not shown in Fig. 6) is deposited to fill up the deep trench 56, and the sacrificial layer (not shown) is etched back to expose a portion of the arsenic silicate glass film 58. Afterward, an anisotropic etching process is performed to remove the exposed arsenic silicate glass film 58 such that a collar region 60 is formed in the inner wall of the deep trench 56. At the same time, a portion of the pad oxide layer 52 is removed during the anisotropic etching process to form a recess 62. Finally another etching process is performed to remove the remaining sacrificial layer (not shown).

[0018] As shown in Fig. 7, a chemical vapor deposition process is performed to form a silicon nitride layer 64 on the inner wall of the deep trench 56, and to fill up the recess 62 with the silicon nitride layer 64 as well. Then a thermal process is performed to diffuse the arsenic ions of the arsenic silicate glass film 58 into the substrate 50, such that a doped region 64 is formed.

[0019] As shown in Fig. 8, an anisotropic etching process is performed by use of hydrofluoric acid (HF) and ethylene glycol (EG) as an etching solution to remove the silicon nitride layer 64 outside the recess 62. Finally, another etching process is performed to remove the arsenic silicate glass film 58 to carry out the deep trench capacitor buried plate of the present invention.

[0020] It has been shown that the prior art method forms a TEOS layer on the inner wall of the deep trench as a barrier layer and performs a thermal process to form an arsenic doped region at the bottom of the deep trench. Nevertheless, TEOS has poor step coverage ability, therefore a void will easily occur in the opening of the deep trench. In addition, the TEOS layer is not able to afford good results as a barrier layer, thus the arsenic ions will easily pass through the TEOS layer and diffuse to the collar region.

[0021] It also has to be noted that the pad oxide layer and the TEOS layer are both composed of silicon oxide, as a result parts of the pad oxide layer will be removed when the TEOS layer is etched. The removal of the pad oxide layer would increase the critical dimension of the deep trench, and further lead to a short circuit between neighboring deep trenches.

[0022] Comparing to the prior art, the method of the present invention forms a silicon nitride layer on the inner wall of the deep trench as a barrier layer. Since silicon nitride has better step coverage ability and better barrier effect than TEOS, the arsenic ions will not diffuse into the collar region of the deep trench. Furthermore, it has to be noted that the method of the present invention forms a recess in the pad oxide layer and fills silicon nitride into the recess as a passivation layer, such that the problem of the deep trench enlargement is prevented.

[0023] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.